

Sub D  
C1  
implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming a channel region in only the first and second portions to adjust the threshold voltage of a transistor;

forming a plurality of gate electrodes on the channel region; and

implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to define separate channel regions from the channel region that are self-aligned to the plurality of gate electrodes.

C2  
Sub D  
21. (Amended) A method of forming a channel region between isolation regions of an integrated circuit substrate, the method comprising:

forming a mask on first and second adjacent isolation regions in an integrated circuit substrate and extending onto an active area between the first and second adjacent isolation regions to define first and second shielded portions of the substrate adjacent to the first and second isolation regions and an exposed portion of the substrate therebetween, the exposed portion of the substrate comprising a first portion where a gate electrode will be subsequently formed and a second portion where a bit line contact will be subsequently formed, the mask exposing only the first and second portions;

implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming a single channel region in only the first and second portions to adjust the threshold voltage of a transistor;

forming a plurality of gate electrodes on the single channel region; and

implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to form first and second spaced apart channel regions from the single channel region.

Please add the following new Claim 24:

C3  
Sub D  
24. (New) A method of forming a channel region between isolation regions of an integrated circuit substrate, the method comprising:

Sub D  
Cmt C3

forming a mask on the isolation region that extends onto a portion of the substrate adjacent to the isolation region to provide a shielded portion of the substrate adjacent to the isolation region and an exposed portion of the substrate spaced apart from the isolation region having the shielded portion therebetween;

implanting ions into the exposed portion of the substrate using the mask as an implant mask, thereby forming a channel region in the exposed portion of the substrate to adjust the threshold voltage of a transistor; then

forming a plurality of gate electrodes on the channel region; and

implanting ions using the plurality of gate electrodes as an implant mask to form source/drain regions associated with the plurality of gate electrodes and to define separate channel regions from the channel region that are self-aligned to the plurality of gate electrodes.